CLAIMS

What is Claimed:

1. A semiconductor memory device comprising:
   a. a silicon substrate;
   b. a peripheral memory region delineated on said substrate, said peripheral memory region having at least one peripheral memory element formed thereon;
   c. a core memory region also delineated on said substrate, said core memory region having at least one set of dual gate core memory structures formed thereon, said dual gate core memory structures comprising a stacked layer arrangement of semiconductor and dielectric material defining respective sidewall portions; and
   d. dual-purpose sidewall spacer structures formed on said respective sidewall portions, said spacer structure being formed from anti-reflective coating material and being used for lithographic patterning and for protecting said stacked layer arrangement during etching operations.

2. A semiconductor memory device, as recited in Claim 1, wherein:
said anti-reflective coating material being selected from an anti-reflective coating material group consisting of silicon oxynitride (SiON), silicon nitride (Si_3N_4), and silicon germanium (SiGe), said material group having anti-reflective optical properties and being compatible with ion implantation and salicidation fabrication processes.

3. A semiconductor memory device, as recited in Claim 2, wherein:
said anti-reflective coating material being deposited in a thickness ranging from 300Å to 1000Å.

4. A semiconductor memory device comprising:

a. a silicon substrate;

b. a peripheral memory region delineated on said substrate, said peripheral memory region having at least one peripheral memory element formed thereon;

c. a core memory region also delineated on said substrate, said core memory region having at least one set of dual gate core memory structures formed thereon, said dual gate core memory structures comprising a stacked layer arrangement of semiconductor and dielectric material defining respective sidewall portions; and

d. dual-purpose spacer structures formed on said respective sidewall portions, said dual-purpose spacer structures being formed from anti-reflective coating material and being selected from an anti-reflective coating material group consisting of silicon oxynitride (SiON), silicon nitride (Si_3N_4), and silicon germanium (SiGe), said material group having anti-reflective optical properties and being compatible with ion implantation and salicidation fabrication processes.

5. A semiconductor memory device, as recited in Claim 4, wherein:

said anti-reflective coating material being deposited in a thickness ranging from 300Å to 1000Å.

6. A method of fabricating a semiconductor memory device, said method comprising the steps of:

a. providing a semiconductor substrate;

b. fabricating core and periphery memory regions on said substrate

c. depositing a first layer of anti-reflective coating material for use in lithographic patterning of said core and periphery memory region;

d. patterning and forming at least one pair of dual gate stacked structures on said core memory region, each one of said dual gate stacked structures having

respective sidewalls;

e. stripping all of said first layer of anti-reflective coating material deposited in said step (c);

f. depositing a second layer of anti-reflective coating material over the dual gate stacked structures on said core memory region and on said periphery memory region after being stripped in accordance with said step (e), said depositing step including depositing said second layer of anti-reflective coating material on said sidewalls and on floor regions between said gate stacked structure and between a core memory and periphery memory interface region;

g. patterning and forming any remaining gate structure on said periphery memory regions; and

h. forming dual-purpose spacer structures on said sidewalls by stripping said second layer of anti-reflective coating material deposited over said floor region, over said interface region, over said dual gate stacked structure and over any formed peripheral gate structure, but not from said sidewalls, said dual-purpose spacer structures being used for lithographic patterning and for protecting said dual gate stacked structure during etching operations.

7. A method of fabricating a semiconductor memory device, as recited in Claim 6, wherein: said step (f) comprises selecting said anti-reflective coating material from an anti-reflective coating material group consisting of silicon oxynitride (SiON), silicon nitride (Si_3N_4), and silicon germanium (SiGe), said material group having anti-reflective optical properties and being compatible with ion implantation and salicidation fabrication processes.

8. A method of fabricating a semiconductor memory device, as recited in Claim 6, wherein said step (h) results in producing a semiconductor memory device, said device comprising:

a. said semiconductor substrate;

b. at least one peripheral memory element formed during said step (g); and

c. at least one set of said dual gate core memory structures having said dual-purpose sidewall spacer structures formed during said step (h).

9. A method of fabricating a semiconductor memory device, as recited in Claim 7, wherein said step (h) results in producing a semiconductor memory device, said device comprising:

a. said semiconductor substrate;

b. at least one peripheral memory element formed during said step (g); and

c. at least one set of said dual gate core memory structures having said dual-purpose sidewall spacer structures formed during said step (h).

10. A method of fabricating a semiconductor memory device, said method comprising the steps of:

a. providing a semiconductor substrate;

b. fabricating periphery memory regions on said substrate, said periphery memory region comprising at least one layer of a semiconductor material formed over said substrate;

c. fabricating core memory regions on said substrate, said core memory regions comprising a layer arrangement of dielectric and semiconductor material;

d. depositing a first layer of anti-reflective coating material over said layer arrangement and over said periphery memory region;

e. patterning at least one pair of dual gate stacked structure on said core memory region, each one of said dual gate stacked structure having respective sidewalls;

f. stripping any first layer of anti-reflective coating material remaining on said dual gate stacked structure and on said periphery memory region;

g. depositing a second layer of anti-reflective coating material over the dual gate stacked structures on said core memory region and on said periphery memory region after being stripped in accordance with said step (f), said depositing step including depositing said second layer of anti-reflective coating material on said sidewalls and on floor regions between gate stacked structure and between core memory and periphery memory interface regions;

h. patterning and forming any remaining gate structure on said periphery memory regions; and

i. forming dual-purpose spacer structures on said sidewalls by stripping said second layer of anti-reflective coating material deposited over said dual gate stacked structure and over any formed peripheral gate structure, but not from said sidewalls, said dual-purpose spacer structures being used for lithographic patterning and for protecting said dual gate stacked structure during etching operations.

11. A method of fabricating a semiconductor memory device, as recited in Claim 10, wherein:

said step (g) comprises selecting said anti-reflective coating material from an anti-reflective coating material group consisting of silicon oxynitride (SiON), silicon nitride (Si_3N_4), and silicon germanium (SiGe), said material group having anti-reflective optical properties and being compatible with ion implantation and salicidation fabrication processes.

12. A method of fabricating a semiconductor memory device, as recited in Claim 10, wherein said step (i) results in producing a semiconductor memory device, said device comprising:

a. said semiconductor substrate;

b. at least one peripheral memory gate structure formed during said step (h); and

c. at least one set of said dual gate core memory structures having said dual-purpose sidewall spacer structures formed during said step (i).

D931

13. A method of fabricating a semiconductor memory device, as recited in Claim 11, wherein said step (i) results in producing a semiconductor memory device, said device comprising:

a. said semiconductor substrate;

b. at least one peripheral memory gate structure formed during said step (h); and

c. at least one set of said dual gate core memory structures having said dual-purpose sidewall spacer structures formed during said step (i).

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